REMARKS

Claims 7-9 were allowed. Claims 2, 5, and 6 were objected to as depending upon rejected base claims. Claims 1, 3, and 4 were rejected as unpatentable over Marko in view of Kost. Applicant requests reconsideration. Claim 2 was amended to include all of the limitations of base claim 1 to traverse the objection, now standing allowable. Claims 3, 4, 5, and 6 were amended to depend on base claim 2, traversing the rejections as to claim 3 and 4, and traversing the objections to claims 5 and 6. As such, claims 2 through 9 are in suitable form for allowance.

Claim 1 stands rejected without amendment. Claim 1 is characterized as having a parallel filter bank comprising a bank of polyphase filters respectively receiving polyphase digital outputs from a parallel A/D converter, and comprising a processor for receiving filtered outputs from the bank of polyphase filters. Marko and Kost do not suggest a parallel filter bank for improved speed of operation and computational efficiency.

Kost describes an analog-to-digital (ADC) conversion system for wideband signals. The system includes a plurality (two) of A/D converters (ADC), a digital-to-analog converter (DAC), and a digital signal conditioning stage. The Kost system permits a sampling rate that is a multiple of a single ADC. The Kost system however does not describe any channelization, but merely uses a plurality (two) of polyphase samplers and converters for providing polyphase digital output. The Kost system then recombines the

polyphase digital outputs into a single signal 57. So, when fairly read, Kost teaches splitting, polyphase staggered sampling, and subsequent combining for increasing the sampling speed. There is no hint of a polyphase filter bank in Kost comprising a bank of polyphase filters and a processor for transforming the filter outputs.

In the present invention, the polyphase ADC 14, including the samplers 34a-m and converters 36a-m provides a plurality of digital outputs that are time staggered. These time-staggered samples are fed directly into a polyphase filter bank 42a-m. Time staggering for purposes of channelization has been performed in the prior art channelizers by internal commutators, not shown in the cited references. The present invention does not include a commutator for channelizing a sampled digital input. Kost teaches staggered sampling for improved speed. Particularly, Kost shows a plurality of staggered signals that are combined. Kost teaches a single combined output. Kost certainly does not suggest using a bank of samplers and converter for eliminating the need of a commutator by feeding the staggered digital outputs into polyphase filters.

Marko teaches a method to separate the received FDMA (Frequency Division Multiple Accessing) signal into individual channels. The system of Marko is comprised of a conversion of the FDMA signal into a complex baseband signal, converting the real and imaginary parts of the resulting signal into digital form and providing individual means for separating the individual channels from the digitized complex baseband signal. The individual means is

comprised of a digital complex-mixer and a pair of digital low pass filters (LPF). The individual means is replicated for each of the individual channels present in the FDMA signal. In the application considered by Marko, there are six channels in the FDMA signal, therefore, the means for separating an individual channel is replicated 6 times as shown in Figure 10 of Marko. Such an arrangement is known as direct implementation and has many disadvantages compared to other implementations. These disadvantages include the need for each of the digital LPFs to operate at full sampling rate of the composite FDMA signal which according to the Nyquist criteria must be at least two times the bandwidth of the FDMA signal. Thus the required sampling rate of the composite signal is equal to the number of channels N multiplied by the required sampling rate for an individual channel. This may not be a critical disadvantage for the application considered by Marko where N is equal to only 6. However, for applications involving hundreds of channels, the required sampling rate is multiplied by a large factor. In addition, each of the digital LPF in Marco's implementation is a full-length filter. For FIR filter implementation, such a filter length M may be equal to a few hundred. Furthermore, Marco's implementation requires a separate digital mixer for each channel. The term wideband is somewhat subjective. In present day terminology, wideband refers to a bandwidth of several hundred megahertz rather than 12.5 MHz used in Marco' application. Thus, the true meaning of wideband in the present context is the bandwidth where the availability, speed and cost of both the individual components and the overall system are important and possibly critical. Marco's application with 12.5 MHz

bandwidth does not have any real need to address these issues as applied to components such as ADC, filters etc. and the total channelizer. Therefore Marko has used the most direct implementation known. The main focus of Marco's invention is the frequency plan selected for the Satellite Digital Audio Radio Service (SDARS) for the XM configuration of two geostationary satellites and terrestrial repeaters so that the mutual interference among the signals from the two satellites and the terrestrial repeater is minimized when processed through the radio receiver.

Marco uses a traditional direct implementation of the digital channelizer and in his patent there is no indication of using a polyphase channelizer or any other channelizer architecture, nor does he show any need or use for a different ADC architecture other than the traditional one. The replacement of the ADC in Marko's system by the ADC taught by Kost will still require that the number of digital filters is equal to twice the number of channels, one for real part and one for imaginary part of the signals, and each operating at the sampling rate of the composite FDMA signal. For example, if there are 500 channels each requiring a sampling rate of 10 Msps, that is, mega samples per second, then the Marco's implementation will require 1000 filters each operating at 5000 Msps or at 5.0 Gsps. This means that each of the 1000 filters must have M (typically a few hundred) multiplication within 0.2 nsec (0.2×10^{-9} sec.) for this example. In contrast, the polyphase system of the present invention will have 1000 filters each operating at only 10Msps rate, and the individual filter length will be only of

the order M/N (1 to 2) in this example, i.e., the number of multiplications for each filter is equal to M/N (1 to 2) in 0.1 μsec (0.1×10^{-6} sec.) thus achieving an overall reduction in the computational rate by a factor of $500 \times 500 = 2.5 \times 10^5$. Thus, there are several orders of improvement in both the size and speed of hardware required. This remarkable improvement is accomplished by a bank of polyphase filters and a transform processor that will be absent in an architecture obtained by replacing the ADC in the Marco's receiver by the ADC architecture taught by Kost as suggested by the examiner. Due to enormous difference in the computational requirements, of about 5 orders of magnitude in the illustrative example, the architecture obtained by replacing the ADC in the Marco's receiver by the ADC architecture taught by Kost will fall short of solving the channelization problem for truly wideband signals with realistic cost, size and weight of the channelizer. These factors are important in most communication applications but especially so in the space based systems. This problem has been solved by the present invention. More specifically, each of the digital component in the present invention includes the sampler, ADC, polyphase filter, and processor operating at a rate determined by single channel in the FDMA signal, i.e., at a rate of 10 Msps in the above example instead of 5000 Msps required by Marko' implementation and yet each of the filters in the polyphase bank has a length of M/500 compared to the filter length of M for each of the 1000 filters in the Marko's implementation. Thus, in the polyphase implementation of the present invention, there are essentially only 2 filters each of length M shared among all of the N channels. These and other

advantages are clearly absent in an architecture obtained by replacing the ADC in the Marco's receiver by the ADC architecture taught by Kost.

Thus, in real practical terms, the architecture obtained by replacing the ADC in the Marco's receiver by the ADC architecture taught by Kost, as suggested by the examiner, will not solve the problem of channelization of truly wideband signals (FDMA bandwidth in hundreds of MHz) with realistic cost, size, power and weight requirements for the channelizer. This is the problem solved by the present invention using the combination of polyphase filters and the transform processor.

In the present invention, the bank of samplers and converters effectively functions as a commutator. The present invention is well deserving of patent protection. The present invention uses polyphase staggered sampling and converting as an extension of Kost and applied to channelization for a new purpose, and that is to perform both high-speed sampling and polyphase commutating during channelization. As such, the bank of samplers and converters are not merely high-speed samplers and converters but become, in effect, a front-end channelizer of channelized digital outputs that can be then fed directly into the bank of u1-m polyphase filters. The polyphase staggered digital outputs from the samplers and converters are directly fed into the u1-m polyphase filter bank 16 without the use of a commutator.

In the preferred form of the present invention, there is a one-to-one and onto mapping between the sampled and converted digital outputs to the u1-m filters and the channelization outputs 48a-m, but other mappings could be used. The present invention provides a full bank of samplers and converters for effective front-end polyphase channelization. In the present invention, the digital outputs to the u1-m filters are at a low rate of the samplers and converters, and as such, the channelization function of the present invention need not operate upon an ultra-high speed single input signal for further cost savings with improved system performance. The present invention not only provides high speed staggered input sampling, as in Kost, but also provides effective channelization by the samplers and converters without the need for commutation, and with polyphase filter banks operating on low sampled rates digital input for improved performance.

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The combination of Marko and Kost does not teach or suggest a bank of polyphase filters and a transform processor for polyphase channelization which will be absent in an architecture obtained by replacing the ADC in the Marco's receiver by the ADC architecture taught by Kost as suggested by the examiner. Allowance of claim 1 as well as claims 2-9 is requested.

Respectfully Submitted

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